A Short Term Analogue Memory

Shah, Peter Jivan

Published in:
Proceedings of the 18th European Solid-State Circuits Conference

Publication date:
1992

Document Version
Publisher's PDF, also known as Version of record

A Short Term Analogue Memory

Peter Shah
Electronics Institute
Building 349
Technical University of Denmark
2800 Lyngby
DENMARK

Abstract

A short term analogue memory is described. It is based on a well-known sample-hold topology in which leakage currents have been minimized partly by circuit design and partly by layout techniques. Measurements on a test chip implemented in a standard 2.4 micron analogue CMOS process show a droop rate of 0.075mV per second with a 1pF hold capacitor. This is equivalent to a retention time of approximately 1½ minute with 10 bits accuracy, assuming a full scale of +/- 3.5V. It is expected that this can be improved by more than an order of magnitude by improving the layout of the hold capacitor. Thus hold times of several hours should be achievable with moderate capacitance values.

Introduction

In a number of analogue memory applications the stored value need not be kept indefinitely, but only "for a long time". E.g in extremely low frequency signal processing a memory element is used for creating long but not infinite time delays, and in real-time learning neural networks the synapse weights need to be stored for a definite period only, since they are updated from time to time by the learning algorithm [1, chapter 8]. On the other hand, the resolution of the weights turns out to be very important - in the networks investigated in [2] a resolution of more than 8 bits was found necessary. Therefore analogue "dynamic RAMs", i.e. memories based on continually refreshing a stored quantized voltage, may not be adequate - at present these can only achieve around 5 bits resolution although 8 bits is deemed possible in the near future [3]. The other alternative, analogue EEPROM-like cells [4] also has some disadvantages: It usually requires special processing steps, high voltages, and long programming sequences.

The circuit proposed in this article is based on the "standard" sample-hold circuit shown in Figure 2, in which hold times long enough to qualify the term "analogue memory" are achieved by minimizing the leakage currents. Also, the circuit is non-quantizing by nature and can therefore, in principle, achieve infinite resolution.

Eliminating leakage currents

The various leakage paths are illustrated in Figure 1. A large part of the leakage current due to generation of electron-hole pairs stems from surface phenomena [5, p. 55] such as crystal faults and dislocations etc. which serve as generation/recombination centres. At the interface between the junction and field oxide, indicated by the dotted circle in Figure 1, these phenomena are particularly pronounced because the field oxide is of much poorer quality than the gate oxide. Therefore it would be desirable to have the junction entirely surrounded by high-quality gate oxide which is achieved by using the circular transistor structure shown in Figure 3. Since the junction is now no longer adjacent to field oxide it cannot be part of a field transistor, and thereby another important leakage path is eliminated, viz. the subthreshold current through the parasitic field transistors.

Figure 3 also shows how the junction leakage is suppressed - the transistor is placed in an N-well biased at the same potential as the transistor source. Thus the source-well diode is biased with zero voltage and consequently the current must also be zero. Unfortunately this method is very sensitive to offset voltages in the voltage follower. This is seen from the equation for the current I_D through the diode:

$$I_D = I_S(e^{V_{ofs}/V_{th}} - 1)$$

I_S is the saturation current and $V_{th} = kT/q = 25.9mV$ is the thermal voltage. To obtain any reasonable leakage current reduction V_{ofs} has to be much smaller than V_{th}, e.g. a leakage reduction of a factor of 10 allows only 2.5mV offset.

Finally there exists a leakage current through the capacitor which will be discussed later.

Voltage follower and switch design

The voltage follower is implemented using a standard two-stage operational amplifier [6, p. 485] and the low offset is obtained partly by using a common centroid inter-digitated structure for the input differential pair and partly by dimensioning the transconductance of the active load transistors to be much less than that of the input transistors. Thereby the input offset is essentially reduced to the threshold voltage mismatch between the two input transistors. In addition, a possibility for external offset adjustment has been added. The high DC gain (>100dB) was obtained simply by using low bias currents and the gain-bandwidth was designed to be approximately 500kHz.

The schematic of the entire sample-hold circuit is shown in Figure 4. Here, also, the switch has been expanded somewhat to take care of the subthreshold leak current through the switch transistor. When the circuit is in hold mode the complementary switch **M4/M5** is on so that the voltage across the circular transistor **M1** is zero and hence also the current through it. Of course the output of the operational amplifier must be isolated from the input voltage; this is ensured by the complementary switch **M2/M3**.

The switch circuit is potentially latchup sensitive because the source-well and drain-well diodes may be momentarily forward-biased during switching transients etc. Therefore it is advisable to surround the well with a substrate guard ring.

Experimental results

The circuit is realized in a standard 2.4μm double metal, double poly, N-well, CMOS process, see chip photo in Figure 6. The hold capacitor C_H is a double-poly capacitor of 1pF and the supply voltages are +/-5V.

For the sake of comparison a standard sample-hold circuit (the basic circuit shown in Figure 2) with the same capacitor value was also put on the chip. In stead of the single transistor shown in the figure, a complementary switch with twice minimum-size rectangular transistors was used.

The measured results are summarized below:

OPAMP gain-bandwidth	450kHz
OPAMP offset (without external compensation)	0.7mV
Analogue memory droop rate with offset compensation	4.5mV/minute
Analogue memory droop rate without offset compensation	4.6mV/minute
Analogue memory hold step	275mV
Standard sample-hold circuit droop rate	42mV/minute
Standard sample-hold circuit hold step	56mV

Possible improvements

Figure 7 shows how the held voltages vary with time. The curves show that an offset of 16mV is needed to achieve approximately zero droop rate. So, the hereby induced junction leakage current cancels another significant leakage path which must either be through the capacitor or due to the generation current. The latter is rejected by exposing the chip to a very slight amount of light, thereby artificially increasing the generation current. This actually *improves* the droop rate, indicating that the main leakage path surprisingly must be the one through the capacitor.

In the present design the capacitor consists of two staggered poly plates which, as shown in the cross-section in Figure 5, gives a substantial region of oxide thinning and convergent field patterns. Both lead to much increased electrical field strength and hence promote leakage. Fortunately, the problem can be solved easily by having the top plate lying completely within the bottom plate. Further improvement may be gained by implementing the capacitor as a MOS gate since the thin oxide then is grown at high temperature from mono-crystalline silicon and therefore of higher quality than the poly-silicon based lower-temperature oxide of a double-poly capacitor. So, a great improvement of the retention time should be obtainable by redesigning the capacitor.

In contrast, the standard sample-hold circuit will not benefit much from a capacitor redesign since the capacitor leakage obviously must be the same in the two circuits and consequently only constitutes a minor part of the total leakage in the standard sample-hold circuit.

Conclusion

Even with the inexpedient layout of the hold capacitor in the present design, it is evident that the techniques applied in the analogue memory circuit have substantially improved the retention characteristics of the standard sample-hold circuit. Further dramatic improvement should be obtainable by a simple redesign of the capacitor, hereby solving the all-overshadowing capacitor leakage problem. The retention period will then be directly proportional to the hold capacitor size, and it should be possible to achieve the very long retention times mentioned in the abstract within realistic capacitor sizes.

Unfortunately the hold step of the analogue memory is somewhat larger than that of the standard sample-hold circuit. This is because of the rather large gate area of the circular switch transistor. It is possible to reduce this to half the value by using minimum length for the transistor in stead of the twice minimum length used on the test chip. Also, increasing the hold capacitor size will help. Alternatively a dummy switch transistor can be introduced along the lines described in [7, p. 95] or an algorithmic approach could be used. In any event, this remains a problem to be solved.

Acknowledgements

I would like to thank Ole Hansen of the Danish Microelectronics Center for valuable discussions during this work.

References

[1] David E. Rumelhart, James L. McClelland, and The PDP Research Group, *Parallel Distributed Processing*, vol. 1, MIT Press, 1986.

[2] Torsten Lehmann, *A Hardware Implementation of the Real-Time Recurrent Learning Algorithm*, 10'th European Conference on Circuit Theory and Design, vol. 2, pp. 431-440.

[3] Christian Björk and Sven Mattison, *Multivalued memory in standard CMOS for weight storing in Neural Networks*, 10'th European Conference on Circuit Theory and Design, vol. 2, pp. 461-468, 1991.

[4] Steven Bibyk and Mohammed Ismail, *Issues in Analog VLSI and MOS Techniques for Neural Computing*, in: Carver Mead and Mohammed Ismail, eds., *Analog VLSI Implementation of Neural Systems*, pp.103-133, Kluwer Academic Publishers, 1989.

[5] S. M. Sze, *Semiconductor Devices, Physics and Technology*, John Wiley and Sons, 1985.

[6] Randall L. Geiger, Phillip E. Allen, and Noel R. Strader, *VLSI Design Techniques for Analog and Digital Circuits*, McGraw-Hill, 1990

[7] Roubik Gregorian and Gabor Temes, *Analog MOS Integrated Circuits for Signal Processing*, John Wiley and Sons, 1986

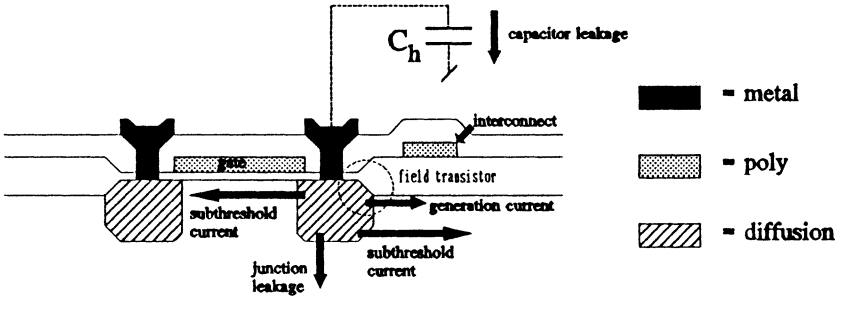

Figure 1 Cross section of the switch transistor with leakage paths.

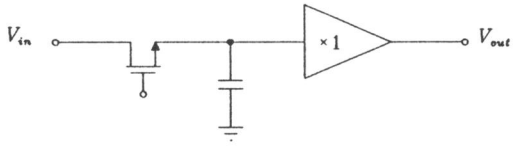

Figure 2 Basic sample-hold circuit.

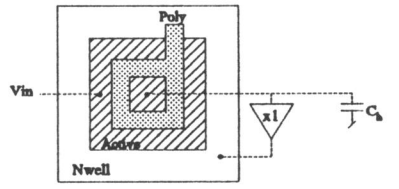

Figure 3 Circular switch transistor structure with suppression of junction leakage by zero-biasing the source-well diode.

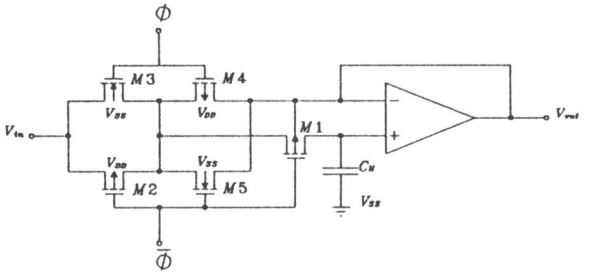

Figure 4 Schematic of the analogue memory.

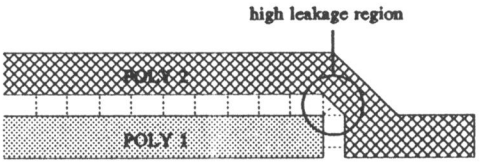

Figure 5 Cross-section of capacitor layout in the present design.

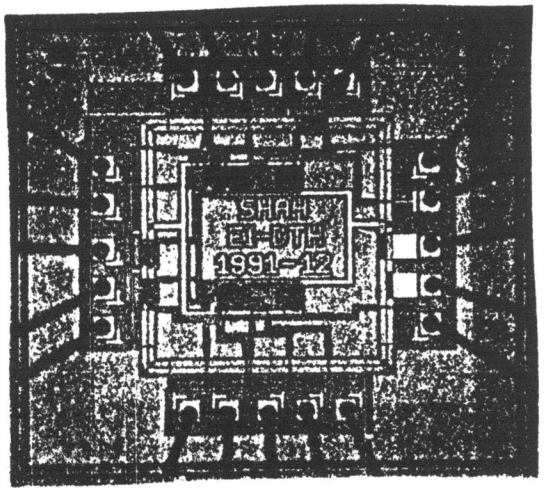

Figure 6 Chip photo.

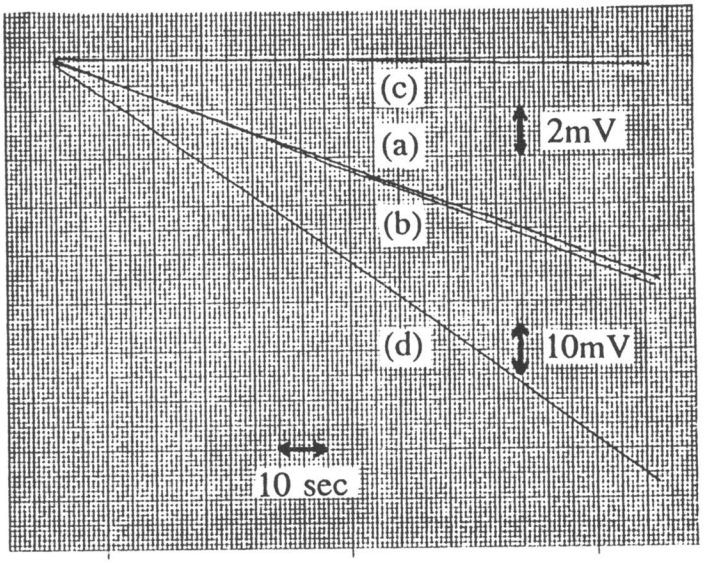

Figure 7 Measured droop versus time in (a) analogue memory with external offset compensation, (b) without compensation, (c) with 16mV offset, and (d) standard sample-hold circuit. Notice the different scale on (d).